REMARKS

Summary of the Office Action

Claims 1-54 are considered in the Office action.

The drawing has been objected to under 37 C.F.R. § 1.84(p)(5) because reference signs mentioned in the description are not included in the drawing.

The specification has been objected to because of lack of clarity. In addition, the Office action states that the use of the trademark VERILOG should be capitalized wherever it appears, and should be accompanied by generic terminology.

Claims 21 and 49 have been objected to because of grammatical errors.

Claims 18, 22-26, 29, 46, 50, 51 and 53 have been rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification in an enabling disclosure.

Claims 1-29 and 31-54 have been rejected under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter of the invention.

Claims 1, 2, 4-10, 30, 31, 32, 34-38 and 54 have been rejected under 35 U.S.C. § 102(b) as anticipated by Steinmetz, Jr. U.S. Patent No. 5,600,579 ("Steinmetz").

Claims 3, 11, 21, 27, 28, 33, 39, 49 and 52 have been rejected under 35 U.S.C. § 103(a) as obvious over Steinmetz in view of "ModelSim EE/PLUS User's Manual, Ver. 5.1, Model Technology, Oct. 1997 ("ModelSim").

Claims 12-17 and 40-45 have been rejected under 35 U.S.C. § 103(a) as obvious over Steinmetz in view of ModelSim and "Tcl Built-In Commands - interp manual page" ("Interp Manual").

Claims 20 and 48 have been rejected under 35 U.S.C. § 103(a) as obvious over Steinmetz in view of ModelSim and "Tcl Built-In Commands - error manual page" ("Error Manual").

Claims 19 and 47 have been rejected under 35 U.S.C. § 103(a) as obvious over Steinmetz in view of ModelSim and IEEE Standard 1364-1995 ("Verilog Standard").

Summary Of Applicant's Response

Applicants have cancelled claims 2-4 and 6-54 without prejudice, and amended claims 1 and 5 to overcome the Examiner's rejections and more particularly point out and distinctly claim the invention.

Reply to the Drawing Objection

The drawing has been objected to under 37 C.F.R. § 1.84(p)(5) because reference signs mentioned in the description are not included in the drawing. Applicants have proposed adding the label "FIG. 1" and reference numerals "10," "20," "100," "110," and "120" to FIG. 1. The corrections to the drawings will be incorporated in the formal drawings if approved by the Examiner.

Reply to Rejection Under 35 U.S.C. § 112

Claims 1-29 and 31-54 have been rejected under § 112, first and second paragraph. Applicants have amended claims 1 and 5 to overcome the Examiner's rejections and more particularly point out and distinctly claim the invention, and have cancelled claims 2-4 and 6-54 without prejudice. Accordingly, applicants respectfully request that the Examiner withdraw the § 112 rejection of claims 1 and 5.

Reply to Rejections Under 35 U.S.C. § 102(b)

Claims 1, 2, 4-10, 30, 31, 32, 34-38 and 54 have been rejected under § 102(b) as anticipated by Steinmetz. Applicants have amended claims 1 and 5 to overcome the Examiner's rejections and more particularly point out and distinctly claim the invention.

Amended independent claim 1 recites a method for providing a design test bench, the method including partitioning functionality of the test bench between a simulation engine and one or more scripted routines, wherein each scripted routine implements a corresponding function, instantiating one or more interpreters in the simulation engine, wherein each interpreter is associated with a corresponding scripted routine and may interact with the simulation engine independently of any other interpreter, causing the simulation engine to pass control to the corresponding interpreter upon encountering one of the functions, and causing the corresponding interpreter to return control to the simulation engine upon encountering a task that is

performed by the simulation engine. Steinmetz does not describe or suggest such methods.

Instead, Steinmetz describes a hardware design verification system including simulator means, test script means and dispatch means. (Col. 3, lines 3-6). In particular, hardware design verification system 100 includes simulation environment 101, test script 103 and dispatch module 105. (Col. 4, line 66 through Col. 5, line 3; Col. 5, lines 21-22; Col. 5, lines 36-37; Col. 5, lines 47-48). Simulation environment 101 provides the resources for modeling the operation of circuit under test 115 and master model 113. (Col. 5, lines 22-27). Test script 103 is designed to test particular features of circuit under test 115. (Col. 5, lines 37-38). Dispatch module 105 bridges the executing test script 103 and simulation environment 101 by forking off the test script and the simulation environment. (Col. 5, lines 47-51). Dispatch module 105 communicates with simulation environment 101 via simulator socket 109 and with test script 103 via test socket 111. (Col. 56-59).

Steinmetz notes that many test scripts 103 can connect to test socket 111 to send and receive packets. In particular, Steinmetz states that "[t]his behavior is possible because sockets can maintain multiple simultaneous connections. This fact means that multiple tests can simultaneously communicate with the simulation environment [101]." (Col. 6, lines 50-53). Unlike the claimed invention, however, Steinmetz does not describe or suggest instantiating one or more interpreters in a simulation engine, wherein each interpreter is associated with a corresponding scripted routine and may interact with the simulation engine independently of any other interpreter. Instead, dispatch module 105 forks multiple test scripts 103 that run concurrently. Steinmetz nowhere describes or suggests that the concurrent test scripts 103 interact independently with simulation environment 101. Indeed, Steinmetz' example VERILOG Master Model, set forth on Col. 23, line 56 through Col. 25, line 10, illustrates this restriction. There is no indication in the example of how it would be possible to connect different stream connections through the same socket to different sections of the VERILOG code.

In addition, Steinmetz does not describe or suggest causing a simulation engine to pass control to a corresponding interpreter upon encountering a function, and causing the corresponding interpreter to return control to the simulation engine upon encountering a task that is performed by the simulation engine. Instead, simulation

environment 101 and test scripts 103 operate concurrently and independently of one another, and do not pass control to one another. (Col. 3, lines 26-29; Col. 3, lines 56-60; Col. 4, line 66 through Col. 5, line 4; Col. 5, lines 59-61). Indeed, dispatch module 105 "is at the heart of the verification system 100 . . . . Its purpose is to bridge the executing test script 103 and the simulation environment 101." (Col. 5, lines 47-49). Further, in Steinmetz' system, "multiple tests can simultaneously communicate with simulation environment [101]." Thus, unlike the claimed invention, Steinmetz does not describe or suggest causing a simulation engine to pass control to a corresponding interpreter upon encountering a function, and causing the corresponding interpreter to return control to the simulation engine upon encountering a task that is performed by the simulation engine.

Because Steinmetz does not describe or suggest the claimed invention, applicants respectfully request that the Examiner withdraw the § 102 rejections of amended independent claim 1. Because claim 5 depends from claim 1, applicants respectfully request that the Examiner withdraw the § 102 rejections of claim 5. Accordingly, applicants respectfully request that the Examiner withdraw the § 102 rejections of claims 1 and 5.

Reply to Rejections Under 35 U.S.C. § 103(a)

Claims 3, 11-17, 19-21, 27, 28, 33, 39-45, 47-49 and 52 have been rejected under 35 U.S.C. § 103(a) as obvious over Steinmetz variously in view of ModelSim, Interp Manual, Error Manual and Verilog Standard. Applicants have cancelled claims 2-4 and 6-54 without prejudice. Accordingly, applicants respectfully submit that the § 103(a) rejections are moot.

Conclusion

For the reasons stated above, applicants submit that this application, including amended claims 1 and 5, is allowable. Applicants therefore respectfully request that the Examiner allow this application.

Respectfully submitted,

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Version of Amended Claims with Markings to Show Changes Made

1. (Amended) A method for providing a [reusable, run time configurable] design test bench, the method comprising:

partitioning functionality of [a] the test bench between a simulation engine and [design verification engine and a scripting language;

implementing a library of] one or more scripted routines [that allow], wherein each scripted routine implements a corresponding function;

instantiating one or more interpreters [to be instantiated in one or more verification engine test benches, wherein said library allows one or more interpreters to be instantiated in a verification engine simulation;] in the simulation engine, wherein each interpreter is associated with a corresponding scripted routine and may interact with the simulation engine independently of any other interpreter;

[said one or more interpreters interacting with said simulation to cause tasks to be executed in said simulation, wherein said simulation starts up an interpreter and instructs it to run a script;

said interpreter passing control back to said verification engine so that said task can be executed when said interpreter encounters a function that is mapped to a certain verification task; and

resuming execution of said one or more scripted routines after executing said task.]

causing the simulation engine to pass control to the corresponding interpreter upon encountering one of the functions; and

causing the corresponding interpreter to return control to the simulation engine upon encountering a task that is performed by the simulation engine.

5. (Amended) The method of Claim 1, [said method] further comprising [:]

synchronizing [said] the simulation engine and [said one or more] the corresponding interpreter[s] via [one or more] a semaphore[s;

wherein control is passed freely between said verification engine and said one or more interpreters].

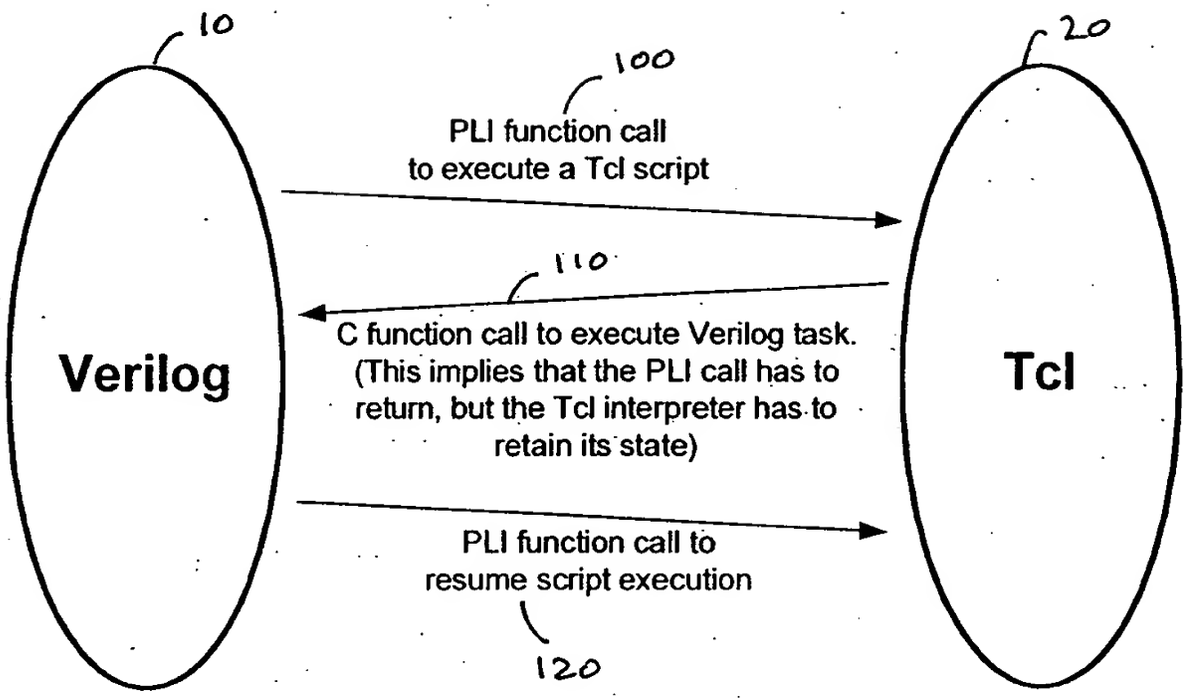

FIG. 1

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